Amendments to the claims:

1 – 11 (Canceled)

12. (Currently amended) The method according to claim ~~9~~ 25 further including the steps of developing deterministic tests, and providing feedback to these deterministic tests, based on the mining and analysis of the simulation traces database.

13 – 20 (Canceled)

21. (New) A system for providing coverage analysis of functional verification of integrated circuit designs comprising:

a) a test specification generator that receives feedback from simulation traces database mining, test program database mining, and coverage database mining modules and generates machine readable test attribute specifications based on said feedback;

b) a test generator that creates test programs using machine readable test attribute specifications, wherein the test programs are developed by the test generator based on specifications that are received from said test specification generator;

c) a simulator that compares the test programs against design model simulations;

d) a database containing traces of simulations generated by functional verification;

e) a program for mining and analyzing the simulation traces database;

f) a database of all test programs generated by the test generators, and by designers and verification engineers;

g) a program for mining and analyzing the test programs database;

h) a database of analysis logs and traces and coverage model results;

i) a program for mining and analyzing the functional coverage database;

j) a program for analysis and monitoring of coverage models;

k) a program for automatic test spec generation from design HDL;

l) a program for test spec adjustment and optimization;

m) a program for creating architectural and microarchitectural coverage models of the test programs; and

n) functional coverage database for storage of the created architectural and microarchitectural coverage models.

22. (New) A system for providing coverage analysis of functional verification of integrated circuit designs comprising:

a) a test generator that creates test programs using machine readable test attribute specifications;

b) a simulator that compares the test programs against design model simulations and stores the simulations in a database, wherein the input to the simulator is based on the development of deterministic tests;

c) a database containing the traces of the simulation generated by the verification process;

d) a program for mining and analyzing the simulation database;

e) a program for mining and analyzing the simulation database including the capability of providing feedback information for tuning the deterministic tests;

f) a database of all test programs generated by the test generators, and by designers and verification engineers;

g) a program for mining and analyzing the test programs database;

h) a database of all functional coverage analysis data and coverage model results;

i) a program for mining and analyzing the functional coverage database;

j) a program for analysis and monitoring of the coverage models;

k) a program for automatic test spec generation from design HDL;

l) a program for test spec adjustment and optimization;

m) a program for creating architectural coverage models of the test programs; and

n) functional coverage database for storage of the created coverage models.

23. (New) A system for providing coverage analysis of functional verification of integrated circuit designs for the purpose of detecting verification trends and patterns to report the same, comprising:

a) a test generator that creates test programs using machine readable test attribute specifications,

b) a simulator that compares the test programs against design model simulations;

c) a simulation database containing the traces of the simulation generated during detection of verification;

d) a program for mining and analyzing the simulation database;

e) a test programs database of all test programs generated by the test generators, and by designers and verification engineers;

f) a program for mining and analyzing the test programs database;

g) a database of all functional coverage analysis data and coverage model results;

h) a program for mining and analyzing the functional coverage database;

i) a program for analysis and monitoring of coverage models;

j) a program for automatic test spec generation from design HDL;

k) a program for test spec adjustment and optimization;

l) a coverage analysis program for creating architectural and microarchitectural coverage models of the test programs;

m) a functional coverage database for storage of the created coverage model, and

n) a coverage report generator based on the information in the functional coverage database and the result of the analysis and mining of the said database wherein the actual verification process trends and patterns discovered are fed back to the test generator, to the architectural and microarchitectural models, to the functional coverage database, and to the coverage report generator.

24. (New) A system for providing coverage analysis of functional verification of integrated circuit designs comprising:

a) a test generator that creates test programs using machine readable test attribute specifications;

b) a simulator that compares the test programs against design model simulations;

c) a database containing the traces of the simulation generated by the verification process;

d) a program for mining and analyzing the simulation database;

e) a database of all test programs generated by the test generators and by designers and verification engineers;

f) a program for mining and analyzing the test program database;

g) a database of all functional coverage analysis data and coverage model results;

h) a program for mining and analyzing the functional coverage database;

i) a program for analysis and monitoring of coverage models;

j) a program for automatic test spec generation from design HDL;

k) a program for test spec adjustment and optimization;

l) a coverage analysis program for creating architectural and microarchitectural coverage models of the test programs;

m) functional coverage database for storage of the created coverage models;

n). a high level description of the design specification for the generation of machine readable coverage analysis models; and

o) a finite state machine and design state event extractor, and a coverage model generator using said machine readable coverage analysis models as input to generate new coverage analysis models or update existing models.

25. (New) A method for coverage analysis of functional verification of integrated circuit designs comprising the steps of:

a) generating test programs based on 1) optimized test specifications and on 2) feedback from analysis and mining of a test programs database, a simulation traces database, and a functional coverage database using machine readable design specifications, and storing the test programs in a database;

b) comparing the test programs against design model simulations to produce simulation traces, and storing the resultant traces in a database;

c) mining and analyzing the test programs database and the simulation traces database;

d) creating architectural coverage models and microarchitectural coverage models; and

e) storing the created models in a functional coverage analysis database.